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Primary Github address: https://github.com/prachi173/da\_sp18

Directory: [https://github.com/prachi173/da\_sp18/tree/master/Design%20Assignments/DA2B](https://github.com/prachi173/da_sp18/tree/master/Design%20Assignments/DA2BA)

Youtube Link: <https://www.youtube.com/watch?v=JVE8w6x-4yc&frags=pl%2Cwn>

The following are required for successful completion of the design assignment:

* 1. a. AVR ASM code that has been compiled and working for all tasks. Verify the period and duty cycle of the waveforms in simulation and emulation.
  2. b. AVR C code that has been compiled and working for all tasks. Verify the period and duty cycle of the waveforms in simulation and emulation.
  3. c. The C code should be well documented with explanation of every instruction.
  4. d. A word document that contains the code with comments, complete schematics, that includes the AVR, components connected on the breadboard and LED should be included. Follow the template provided.
  5. e. A snapshot of the board with connected components and a video of the complete LED bar blink sequence should be recorded and uploaded to Youtube and the line to be provided for each task.
  6. f. The git directory should have DA2C\DA2T1, DA2C\DA2T2, … \_folders, with one doc file and video link file.

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| /\*  \* DA2B\_C.c  \*  \* Created: 3/9/2019 12:56:24 PM  \* Author : patel  \*/  #include <avr/io.h>  #include <avr/interrupt.h>  #define F\_CPU 8000000UL  #include <util/delay.h>  int main(void)  {  DDRB |= (1<<2); //output PB2  PORTB = 0x00; //set leds off    DDRD &= (0<<2); //set pd2 to input  PORTD |= (1<<2); //set portd to enable pind2    EICRA = 0x02; //set falling edge interrupt request  EIMSK = (1<<INT0); //enable int0 through mask register  sei(); //enable interrupts  while (1);  }  ISR (INT0\_vect) //interrupt function  {  PORTB |= (1<<2);  \_delay\_ms(1250);  PORTB = 0x00;  } |
| ;  ; DA2B\_ASM.asm  ;  ; Created: 3/9/2019 4:53:11 PM  ; Author : patel  ;  ; Replace with your application code  .org 0  jmp top  .org 0x02 ;interrupt subroutine origin  JMP EX0\_ISR  top:  LDI R20, HIGH(RAMEND)  OUT SPH, R20  LDI R20, LOW(RAMEND)  OUT SPL, R20 ;intialize the stack  LDI R16, 0x00  SBI DDRB, 2 ;set output port pb.2  SBI PORTD, 2 ;set portd2 high  LDI R20, 0x2  STS EICRA, R20 ;set interrupt request at falling edge  OUT PORTB, R16 ;set all leds off  LDI R20, 1<<INT0 ;set INT0 to enable and load into R20  OUT EIMSK, R20 ;mask register INT0  SEI ;enable interrupt  RJMP top  EX0\_ISR: ;set interrupt functions  LDI R16, 0x04  OUT PORTB, R16 ;output led3 or pb2  ;call delay subroutine  rcall delay\_1s  rcall delay\_100ms  rcall delay\_100ms  rcall delay\_50ms  ;set leds off again  LDI R16, 0x00  OUT PORTB, R16  RETI ;exit interrupt function  ;DELAY SUBROUTINE  delay\_100ms:  push r17  ldi r17, 100  l2:  rcall delay\_1ms  dec r17  brne l2  pop r17  ret  delay\_50ms:  push r22  ldi r22, 50  l3:  rcall delay\_1ms  dec r22  brne l3  pop r22  ret  delay\_1s:  push r19  ldi r19, 10  l4:  rcall delay\_100ms  dec r19  brne l4  pop r19  ret  delay\_1ms:  push r16  push r17  ldi r16, 11  ldi r17, 99  l1:  dec r16  brne l1    l12:  dec r17  brne l12  pop r16  pop r17  ret |
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Verification using a logic analyzer:

~1.25s

A screenshot of a cell phone

Description automatically generated

**Student Academic Misconduct Policy**

<http://studentconduct.unlv.edu/misconduct/policy.html>

“This assignment submission is my own, original work”.

Prachi Patel